[FIG. 1]

1: THREE-PHASE POWER SOURCE

2: INPUT FILTER

3: BIDIRECTIONAL SWITCH GROUP

4: INPUT POWER VOLTAGE PHASE/MAGNITUDE DETECTOR

5: INPUT VOLTAGE VALUE

6: INPUT VOLTAGE PHASE

7: CONTROLLER

8: DRIVE CIRCUIT

9: PWM CYCLOCONVERTER CONTROL UNIT

L1, L2, L3: LOAD

[FIG. 2]

A1: DETAILED DIAGRAM FOR INPUT POWER VOLTAGE PHASE/MAGNITUDE DETECTOR 4

A2: POWER VOLTAGE

41: INPUT VOLTAGE PHASE DETECTION CIRCUIT

42: ARTIFICIAL DC BUS VOLTAGE DETECTION CIRCUIT

43: INPUT VOLTAGE EFFECTIVE VALUE DETECTION CIRCUIT

44: IDEAL INPUT VOLTAGE CALCULATOR

45: INPUT VOLTAGE UPPER AND LOWER LIMIT CALCULATOR

46: VOLTAGE VALUE COMPARATOR

5: INPUT VOLTAGE VALUE

6: INPUT VOLTAGE PHASE

[FIG. 3]

A1: INPUT VOLTAGE

A2: MAXIMUM VALUE AND MINIMUM VALUE OF INPUT VOLTAGE

A3: MAXIMUM VALUE Vmax

A4: MINIMUM VALUE Vmin

A5: ARTIFICIAL DC BUS VOLTAGE

A6: INPUT VOLTAGE PHASE

A7: 360 DEGREES

A8: 0 DEGREE

A9: INTERVAL

[FIG. 4]

A1: INTERVAL 1, ENLARGED

A2: INTERVAL 1

[FIG. 5]

A1: CARRIER WAVE

A2: VOLTAGE COMMAND

A3: INTER-OUTPUT LINE VOLTAGE

[FIG. 6]

1: THREE-PHASE POWER SOURCE

2: INPUT FILTER

3: BIDIRECTIONAL SWITCH GROUP 3 AND PWM CYCLOCONVERTER CONTROL UNIT 9

L1 TO L3: LOAD

11: THYRISTOR INPUT FILTER

12: THYRISTOR

L4: THYRISTOR LOAD

13: PWM CONVERTER INPUT FILTER

14: PWM CONVERTER

15: INVERTER

L5: INVERTER LOAD

[FIG. 7]

A1: PHASE VOLTAGE (IDEAL VALUE)

A2: PHASE VOLTAGE (ACTUAL VOLTAGE VALUE)

A3: INTERVAL

[FIG. 8]

A1: PHASE VOLTAGE (IDEAL VALUE)

A2: PHASE VOLTAGE (ACTUAL VOLTAGE VALUE)

A3: INTERVAL

[FIG. 9]

A1: PHASE VOLTAGE (IDEAL VALUE)

A2: PHASE VOLTAGE (ACTUAL VOLTAGE VALUE)

A3: ARTIFICIAL DC BUS VOLTAGE

A4: INTERVAL

[FIG. 10]

A1: UPPER LIMIT VOLTAGE VALUE

A2: LOWER LIMIT VOLTAGE VALUE

A3: INTERVAL

5: INPUT VOLTAGE VALUE

[FIG. 11]

A1: UPPER LIMIT VOLTAGE VALUE

A2: LOWER LIMIT VOLTAGE VALUE

A3: INTERVAL

5: INPUT VOLTAGE VALUE

[FIG. 12]

A1: POWER VOLTAGE

41: INPUT VOLTAGE PHASE DETECTION CIRCUIT

42: ARTIFICIAL DC BUS VOLTAGE DETECTION CIRCUIT

43: INPUT VOLTAGE EFFECTIVE VALUE DETECTION CIRCUIT

44: IDEAL INPUT VOLTAGE CALCULATOR

45: INPUT VOLTAGE UPPER AND LOWER LIMIT CALCULATOR

46: VOLTAGE VALUE COMPARATOR

47: INPUT VOLTAGE ABNORMALITY DETECTION CIRCUIT

5: INPUT VOLTAGE VALUE

6: INPUT VOLTAGE PHASE

9: POWER VOLTAGE ABNORMAL SIGNAL

[FIG. 13]

A1: POWER VOLTAGE

41: INPUT VOLTAGE PHASE DETECTION CIRCUIT

42: ARTIFICIAL DC BUS VOLTAGE DETECTION CIRCUIT

5: INPUT VOLTAGE VALUE

6: INPUT VOLTAGE PHASE

[FIG. 14]

A1: START

A2: INTERVAL

A3: END

A4: PHASE VOLTAGE

[FIG. 15]

122: POWER VOLTAGE DETECTOR

123: CONTROLLER

124: GATE SIGNAL SYNTHESIZER

125: GATE DRIVER

130: INPUT VOLTAGE INFORMATION DETECTOR

150: PROTECTION GATE SIGNAL GENERATOR

A1: POWER VOLTAGE INSTANTANEOUS VALUE

A2: POWER VOLTAGE PHASE

A3: OUTPUT VOLTAGE COMMAND

[図1]

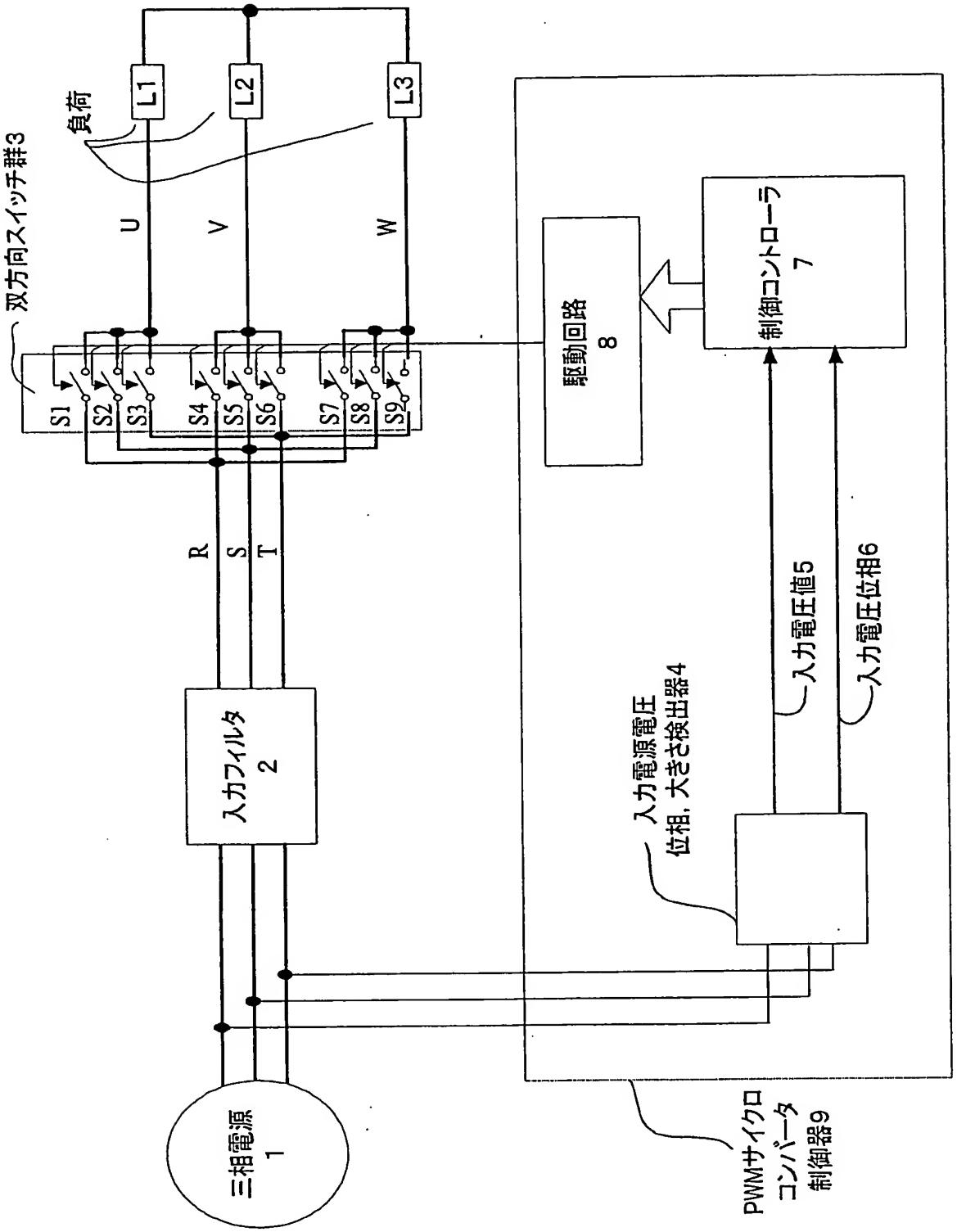
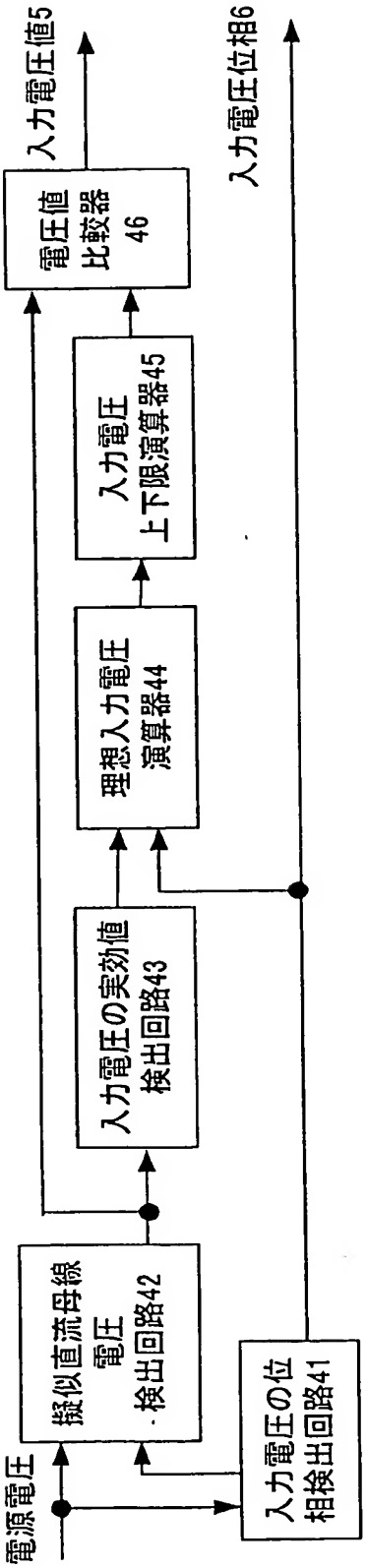


Fig. 1

~~[図2]~~

Fig. 2

入力電源電圧位相，大きさ検出器4の詳細図



[図3]

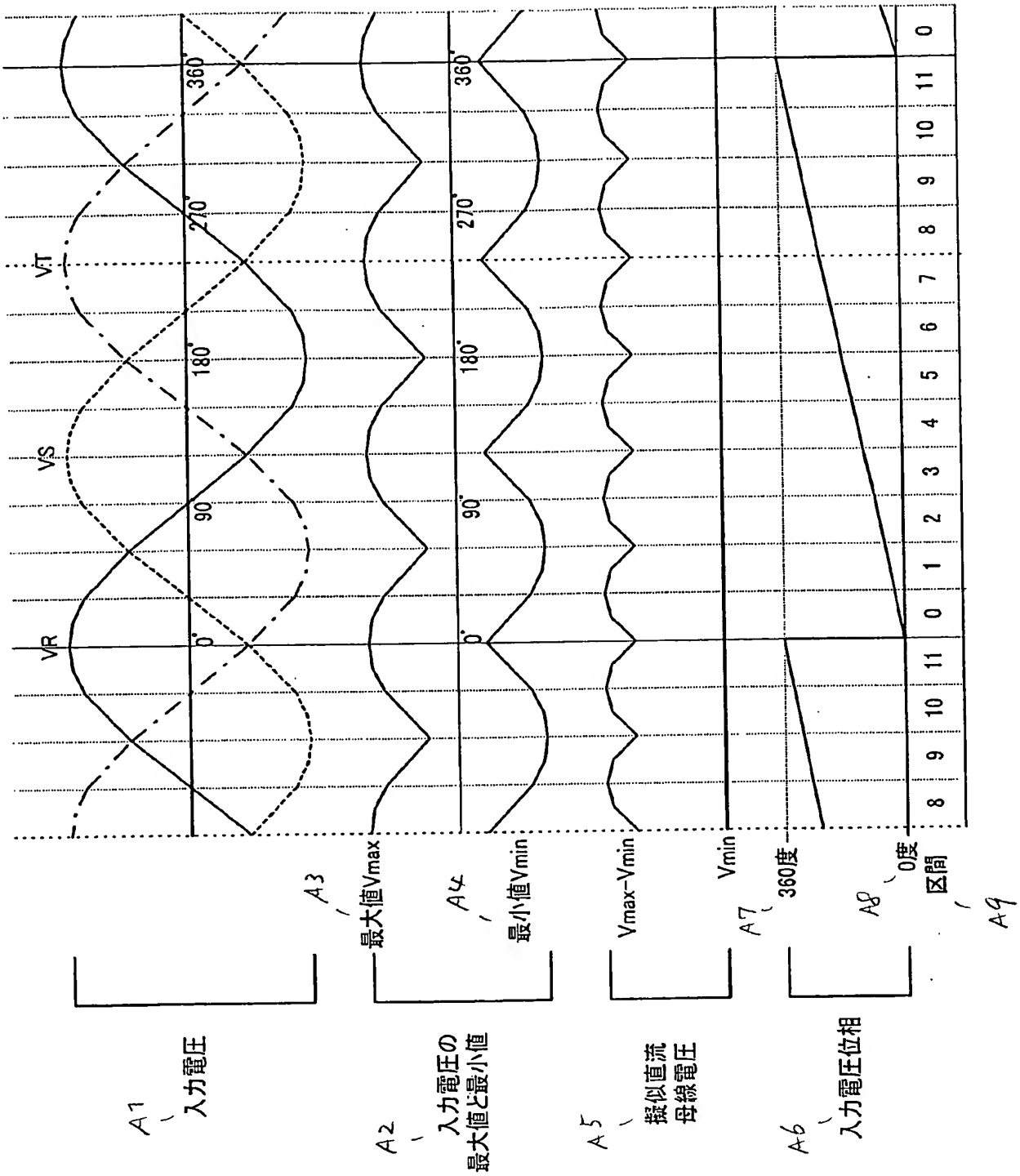


Fig. 3

[図4]

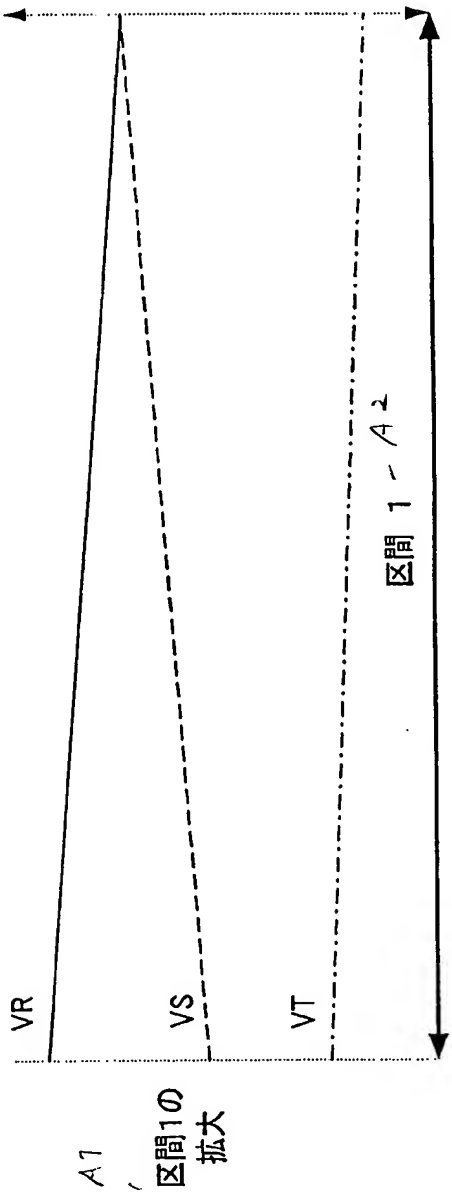


Fig. 4

[図5]

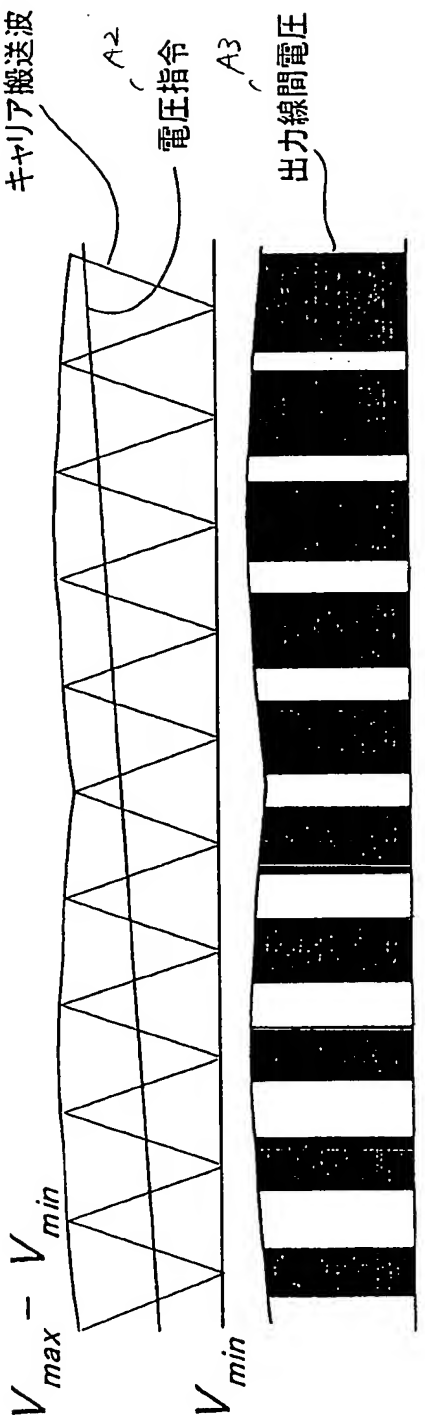


Fig. 5

~~[図6]~~

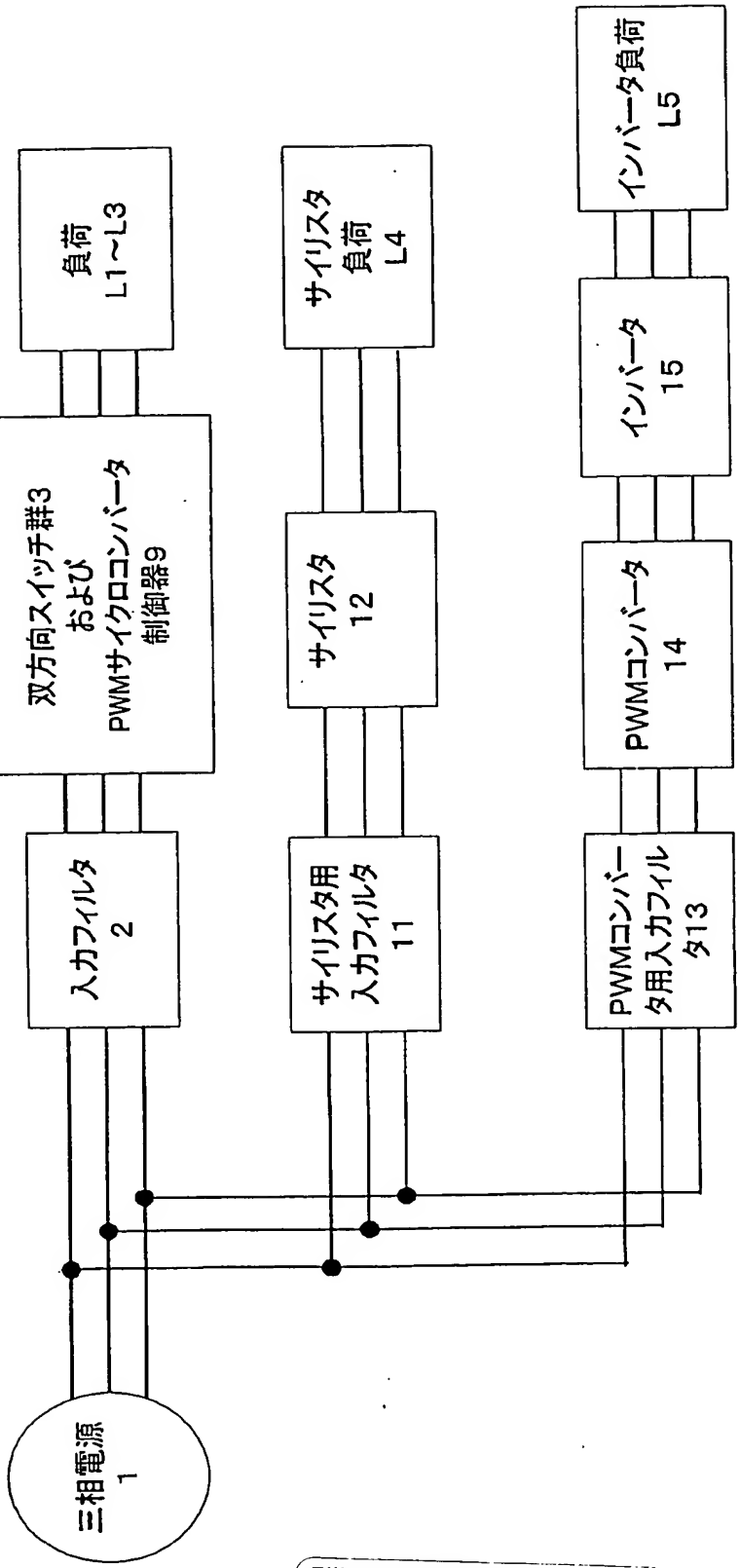


Fig. 6

[図7]

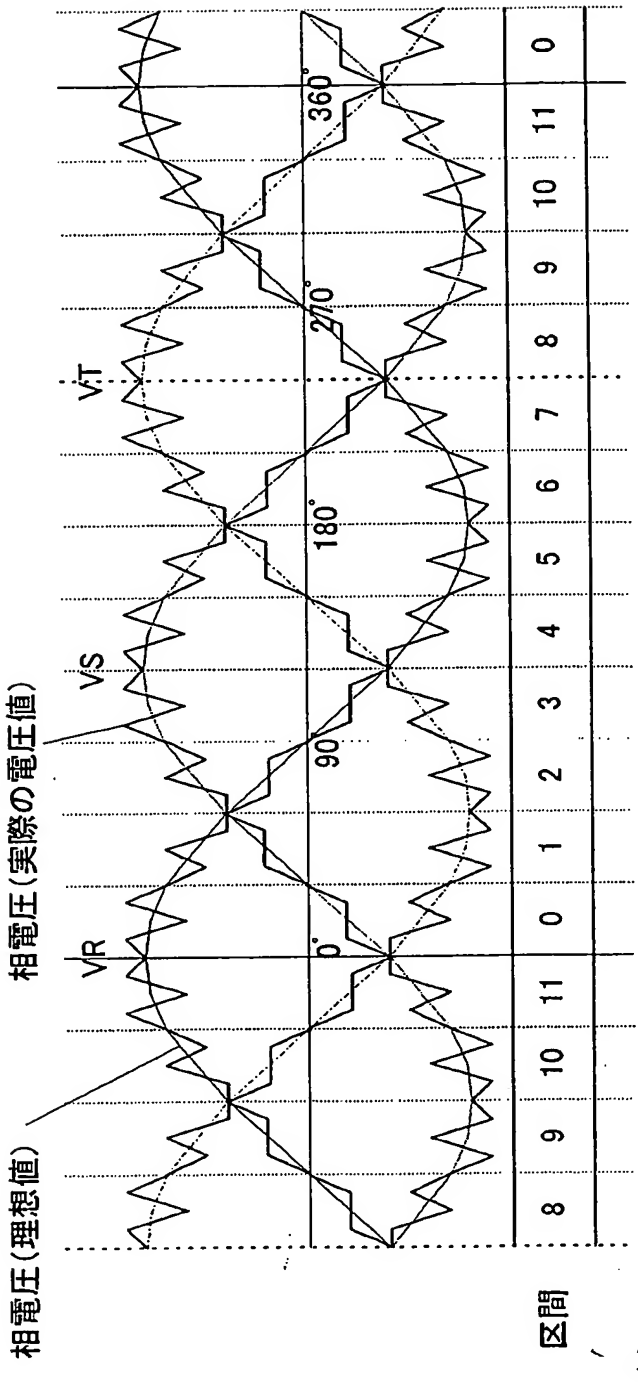

相電圧(実際の電圧値)
相電圧(理想値)
VR
VS
VT
0°
90°
180°
270°
360°
0
1
2
3
4
5
6
7
8
9
10
11
区間
A1
A2
A3

Fig. 7

[図8]

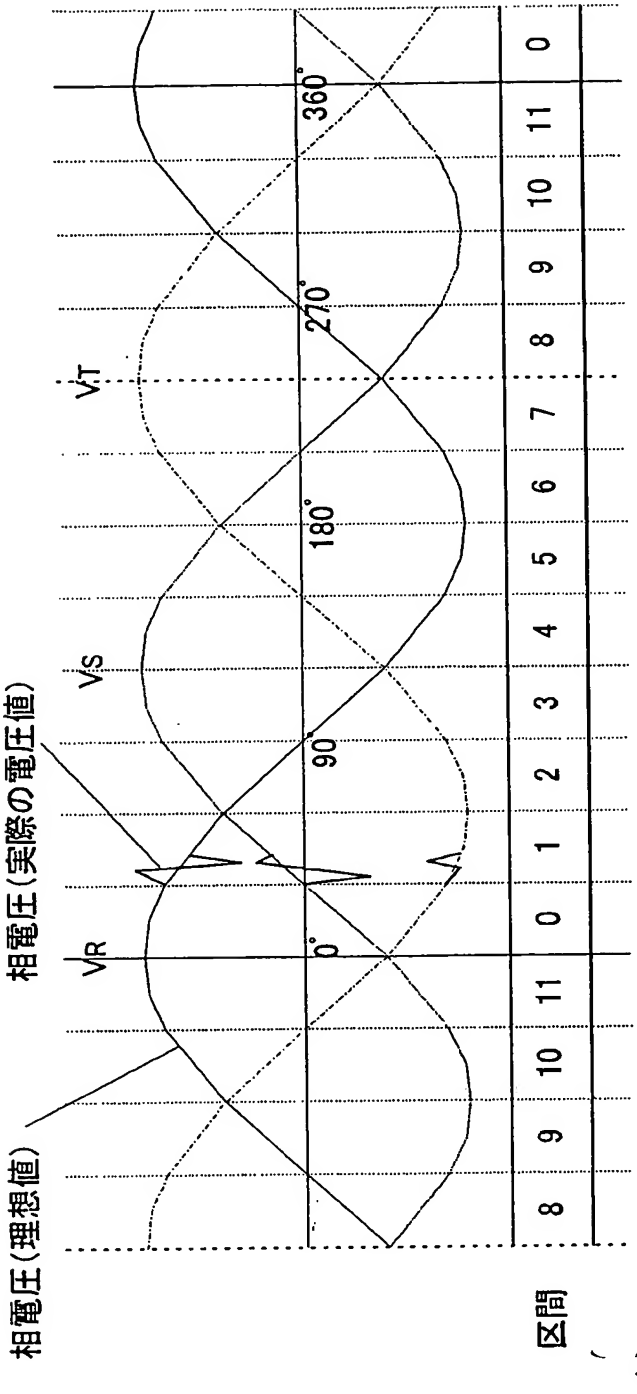


Fig. 8

[図9]

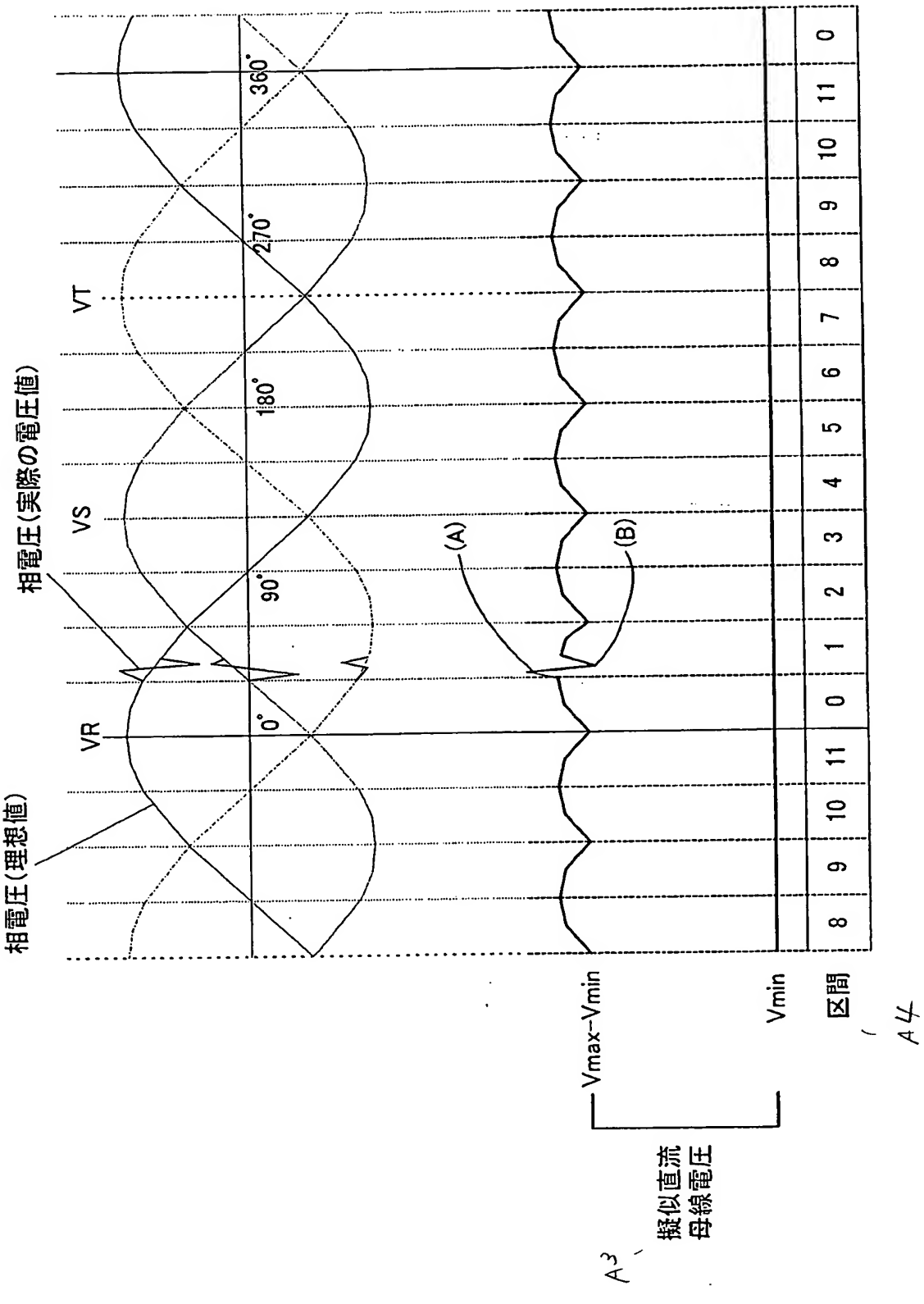


Fig. 9

[図10]

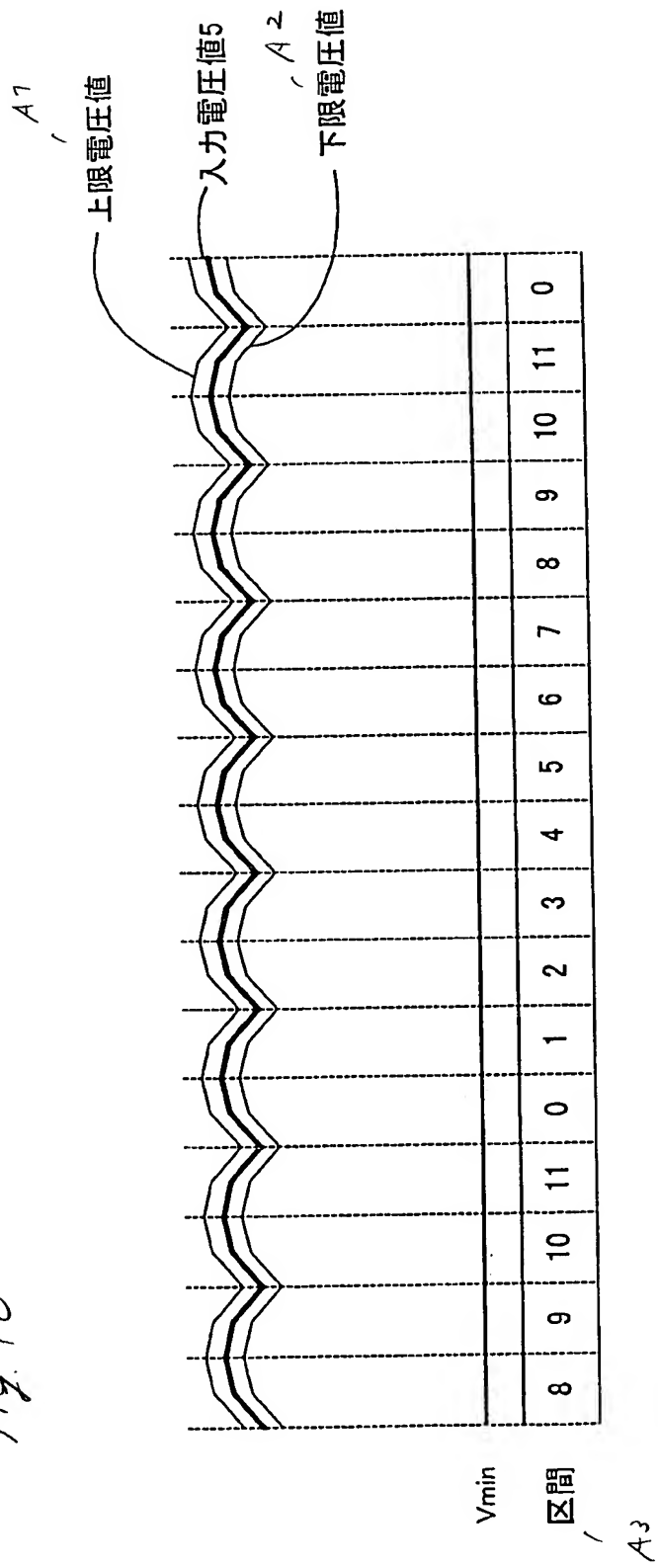


Fig. 10

[図11]

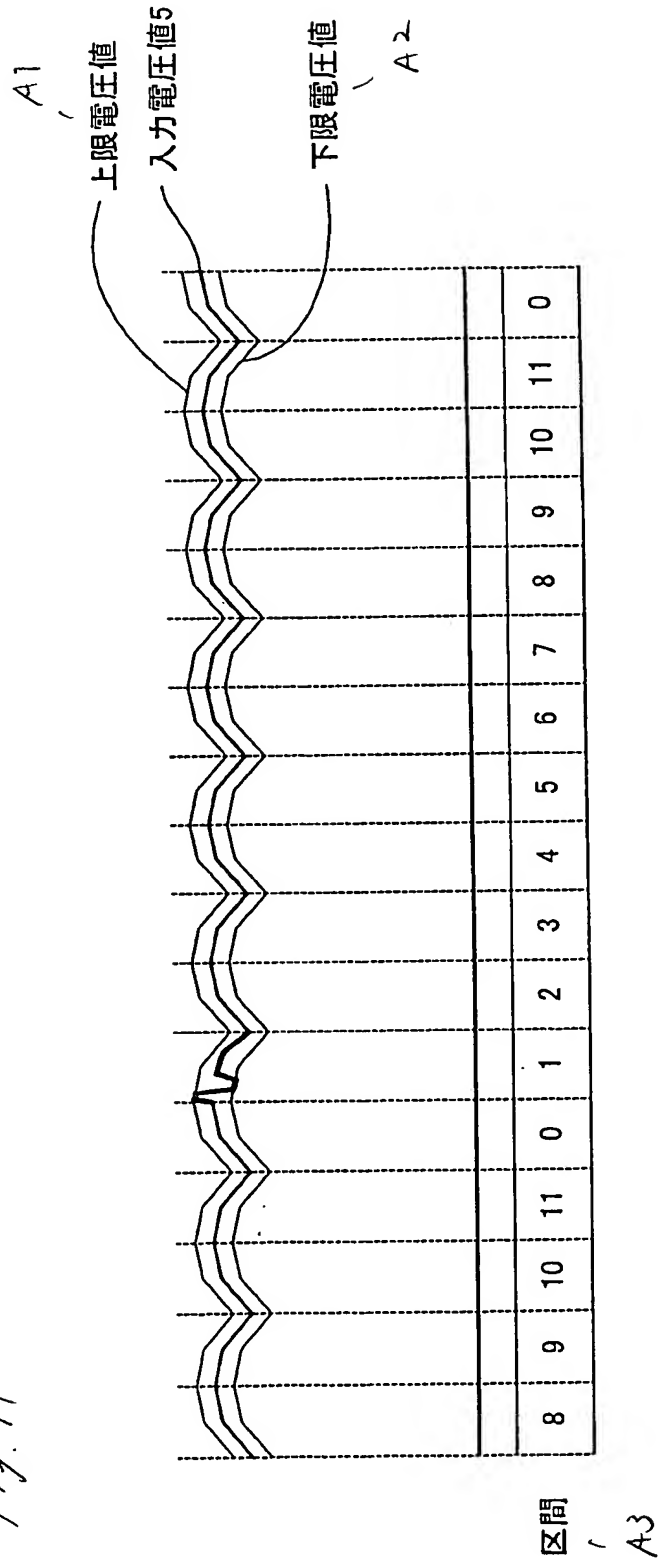


Fig. 11

[図12]

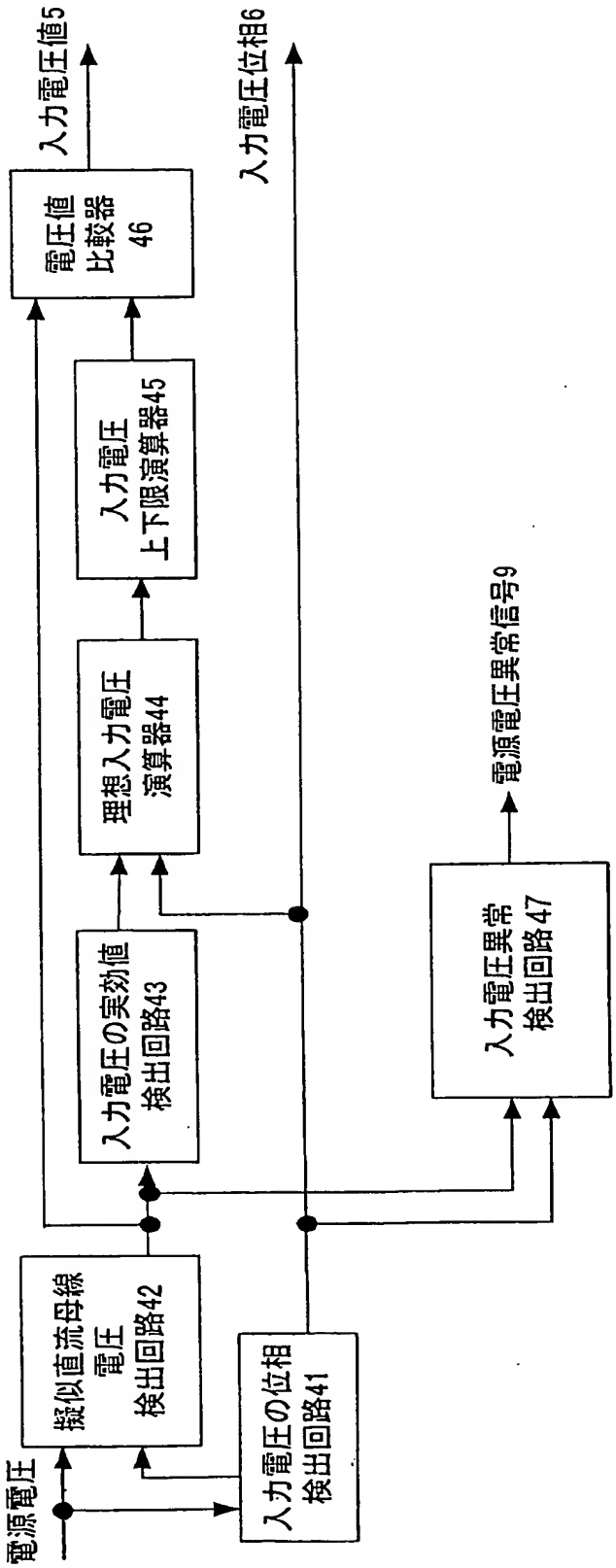
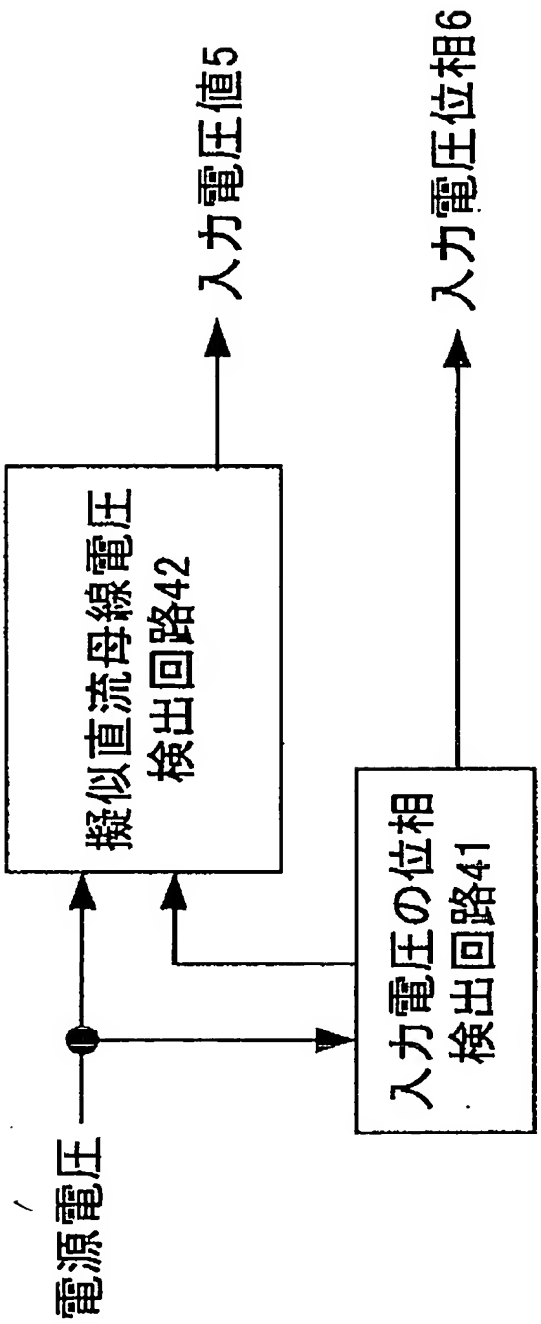


Fig. 12

A1

~~[図13]~~

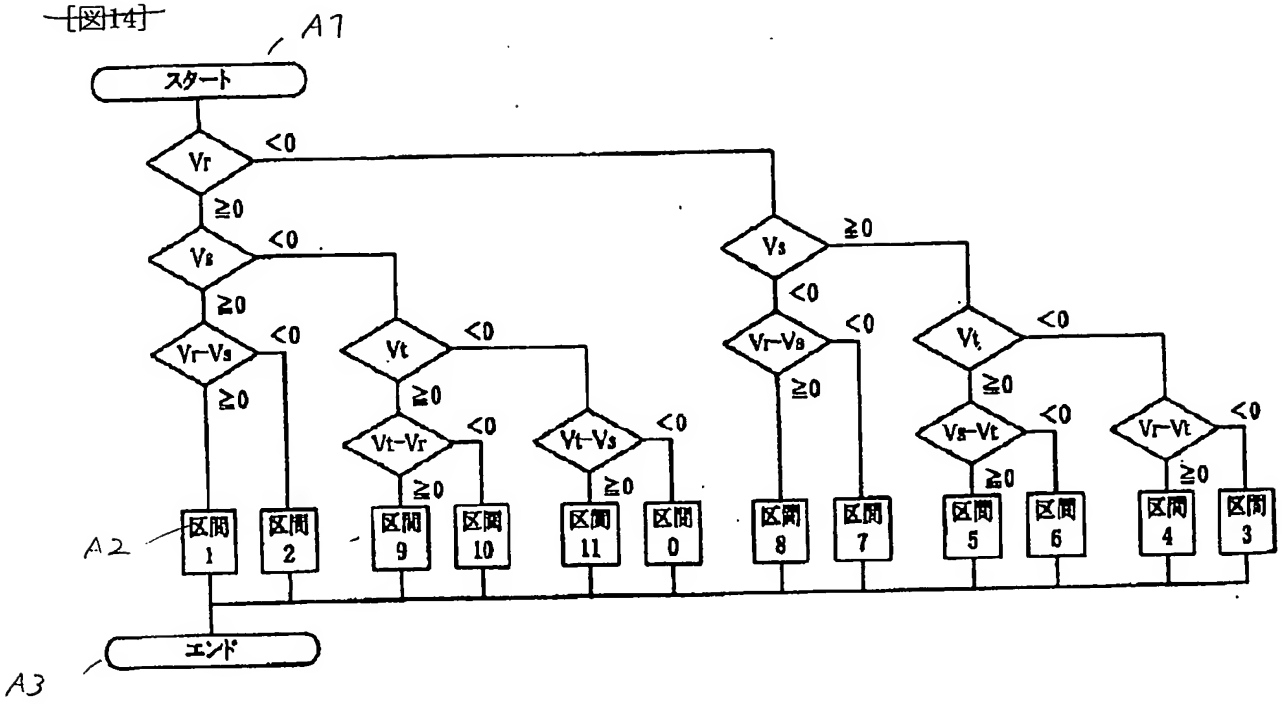


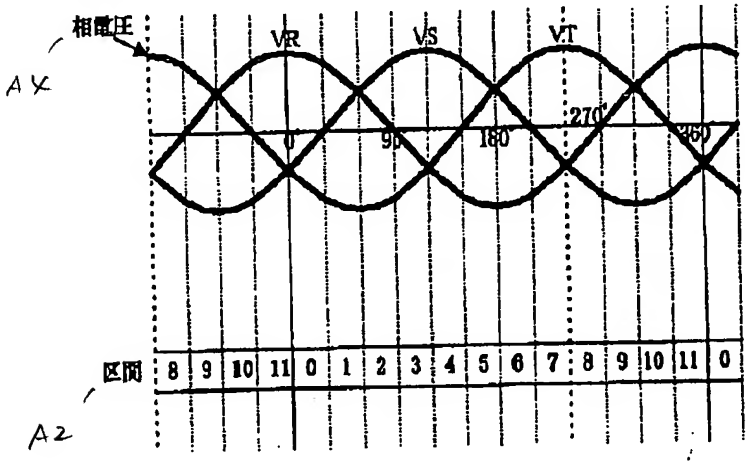
A7

Fig. 13

Fig. 14

[図14]


A1
スタート
Vr
<0
≧0
Vs
Vr-Vs
Vt
Vt-Vr
Vt-Vs
Vs
Vr-Vs
Vt
Vs-Vt
Vr-Vt
区間 1
区間 2
区間 9
区間 10
区間 11
区間 0
区間 8
区間 7
区間 5
区間 6
区間 4
区間 3
A2
エンド
A3


相電圧
A4
VR
VS
VT
0
90
180
270
360
区間
8 9 10 11 0 1 2 3 4 5 6 7 8 9 10 11 0
A2

~~[図15]~~ Fig. 15